AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A semiconductor integrated circuit comprising:

a power supply wiring;

a ground wiring; and

a decoupling capacitor formed between said power supply wiring and said ground wiring, said decoupling capacitor having electrodes,

wherein at least one of the electrodes of said decoupling capacitor comprises a shield layer formed in a plane shape on a semiconductor substrate, and said shield layer is electrically connected ~~electrically~~ directly to said ~~the~~ semiconductor substrate via a diffusion layer, such that a plane shaped portion of said shield layer contacts said diffusion layer, said ~~the~~ shield layer is fixed to a power supply potential or said ~~the~~ ground potential, and said decoupling capacitor does not overlap said diffusion layer,

wherein said at least one of said electrodes comprising said shield layer is extended into said decoupling capacitor while being in a same plane as said plane shaped portion that contacts said diffusion layer.

2. (previously presented): The semiconductor integrated circuit as claimed in claim 1, wherein, another of the electrodes of said decoupling capacitor, which opposes the electrode comprising said shield layer, includes a wiring layer connected to wirings on an uppermost layer

of a multilayer wiring structure via contact electrodes, and a capacitor insulating film for forming said decoupling capacitor is provided between said wiring layer and said shield layer.

3. (currently amended): A semiconductor integrated circuit comprising:

a power supply wiring;

a ground wiring; and

a decoupling circuit formed between said power supply wiring and said ground wiring, said decoupling circuit having electrodes,

wherein at least one electrode of said decoupling circuit comprises a shield layer obtained by covering a plurality of protrusions formed on a semiconductor substrate, and said shield layer is electrically connected directly to the semiconductor substrate via a diffusion layer, such that a plane shaped portion of said shield layer contacts said diffusion layer, ~~the~~ said shield layer is fixed to a power supply potential or ~~the~~ said ground potential, and said decoupling circuit does not overlap said diffusion layer,

wherein said at least one of said electrodes comprising said shield layer is extended into said decoupling circuit while being in a same plane as said plane shaped portion that contacts said diffusion layer.

4. (previously presented): The semiconductor integrated circuit as claimed in claim 3, wherein said protrusions are formed simultaneously with a gate electrode by a same formation process used for the gate electrode.

5. (previously presented): The semiconductor integrated circuit as claimed in claim 1, wherein said decoupling capacitor is formed on an element isolation oxide film.

6. (previously presented): The semiconductor integrated circuit as claimed in claim 1, wherein said shield layer comprises a silicon compound of a metal.

7. (previously presented): The semiconductor integrated circuit as claimed in claim 3, wherein said decoupling circuit is formed on an element isolation oxide film.

8. (previously presented): The semiconductor integrated circuit as claimed in claim 3, wherein said shield layer comprises a silicon compound of a metal.

9. (previously presented): The semiconductor integrated circuit as claimed in claim 1, wherein said diffusion layer is a well contact diffusion layer.

10. (previously presented): The semiconductor integrated circuit as claimed in claim 3, wherein said diffusion layer is a well contact diffusion layer.

11. (previously presented): The semiconductor integrated circuit as claimed in claim 1, wherein said semiconductor substrate includes a p-well region and an n-well region.

12. (previously presented): The semiconductor integrated circuit as claimed in claim 3, wherein said semiconductor substrate includes a p-well region and an n-well region.

13. (new): The semiconductor integrated circuit as claimed in claim 1, wherein said decoupling capacitor is located opposite side with reference to a near gate electrode formed on said semiconductor substrate.

14. (new): A semiconductor integrated circuit comprising:

a power supply wiring;

a ground wiring; and

a decoupling capacitor formed between said power supply wiring and said ground wiring, said decoupling capacitor having electrodes,

wherein at least one of electrodes of said decoupling capacitor comprises a shield layer formed in a plane shape on a semiconductor substrate, and said shield layer is electrically connected directly to said semiconductor substrate via a diffusion layer, such that a plane shaped portion of said shield layer contacts said diffusion layer and is a lowermost conductive layer on said semiconductor substrate, said shield layer is fixed to a power supply potential or said ground potential, and said decoupling capacitor does not overlap said diffusion layer and is located adjacent to said diffusion layer.

15. (new): The semiconductor integrate circuit as claimed in claim 14, wherein, another of said the electrodes of said decoupling capacitor, which opposes said the electrode comprising said

shield layer, includes a wiring layer connected to wirings on an uppermost layer of a multilayer wiring structure via contact electrodes, and a capacitor insulating film for forming said decoupling capacitor is provided between said wiring layer and said shield layer.

16. (new): The semiconductor integrated circuit as claimed in claim 14, wherein said decoupling capacitor is formed on an element isolation oxide film.

17. (new): The semiconductor integrated circuit as claimed in claim 14, wherein said shield layer comprises a silicon compound of a metal.

18. (new): The semiconductor integrated circuit as claimed in claim 14, wherein said diffusion layer is a well contact diffusion layer.

19. (new): The semiconductor integrated circuit as claimed in claim 14, wherein said semiconductor substrate includes a p-well region and an n-well region.